## ABSTRACT OF THE DISCLOSURE

Prediction of a clock skew for an incomplete integrated circuit design, includes (a) selecting a first metal layer having at least one clock design figure, (b) placing, for a minimum clock skew prediction, clock source locations on the clock design figure in accordance with a first predetermined minimum distance between adjacent clock source locations, (c) placing, for a maximum clock skew prediction, a clock source location on a largest clock design figure in the first layer, such that the clock source location has a largest distance from a via to a lower layer, and (d) placing, for an intermediate clock skew prediction, clock source locations on intersections between the clock design figure and a virtual clock grid created for the first metal layer, the virtual clock grid having a predetermined offset from a design boundary and a predetermined pitch between grid lines.